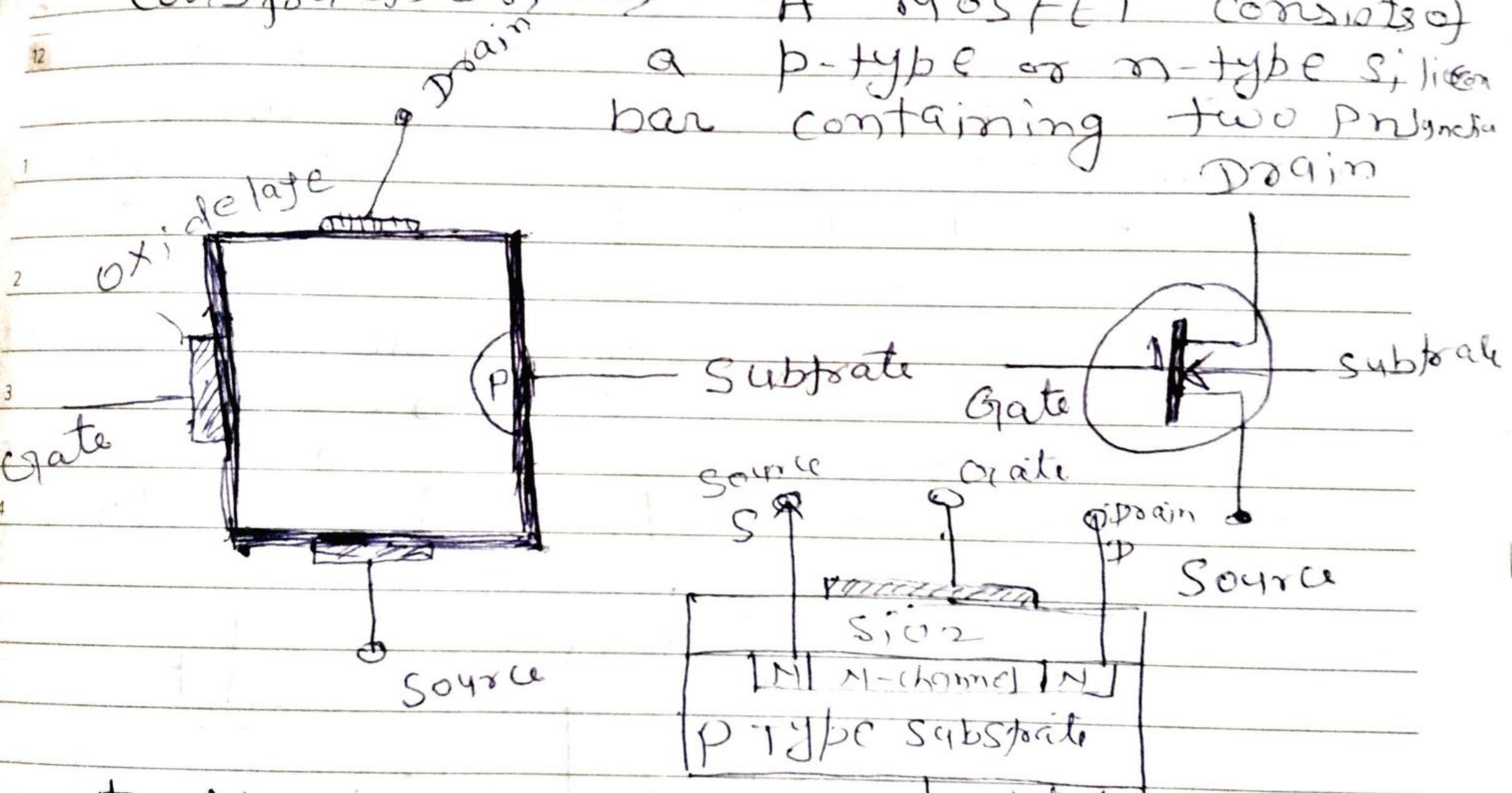


MOSFET

Metal oxide Semiconductor FET

MOSFET is an important semiconductor device. The input impedance of a MOSFET is much more than that of a FET because of very small gate leakage current.

Construction → A MOSFET consists of a p-type or n-type silicon bar containing two PN junctions.



at the sides, the bar forms the conducting channel for the charge carriers. the n channel consists of bar of n-type it has only a single p-region. This region is called substrate.

(ii) A thin layer of metal oxide (usually silicon dioxide) is deposited over the left side of the channel.

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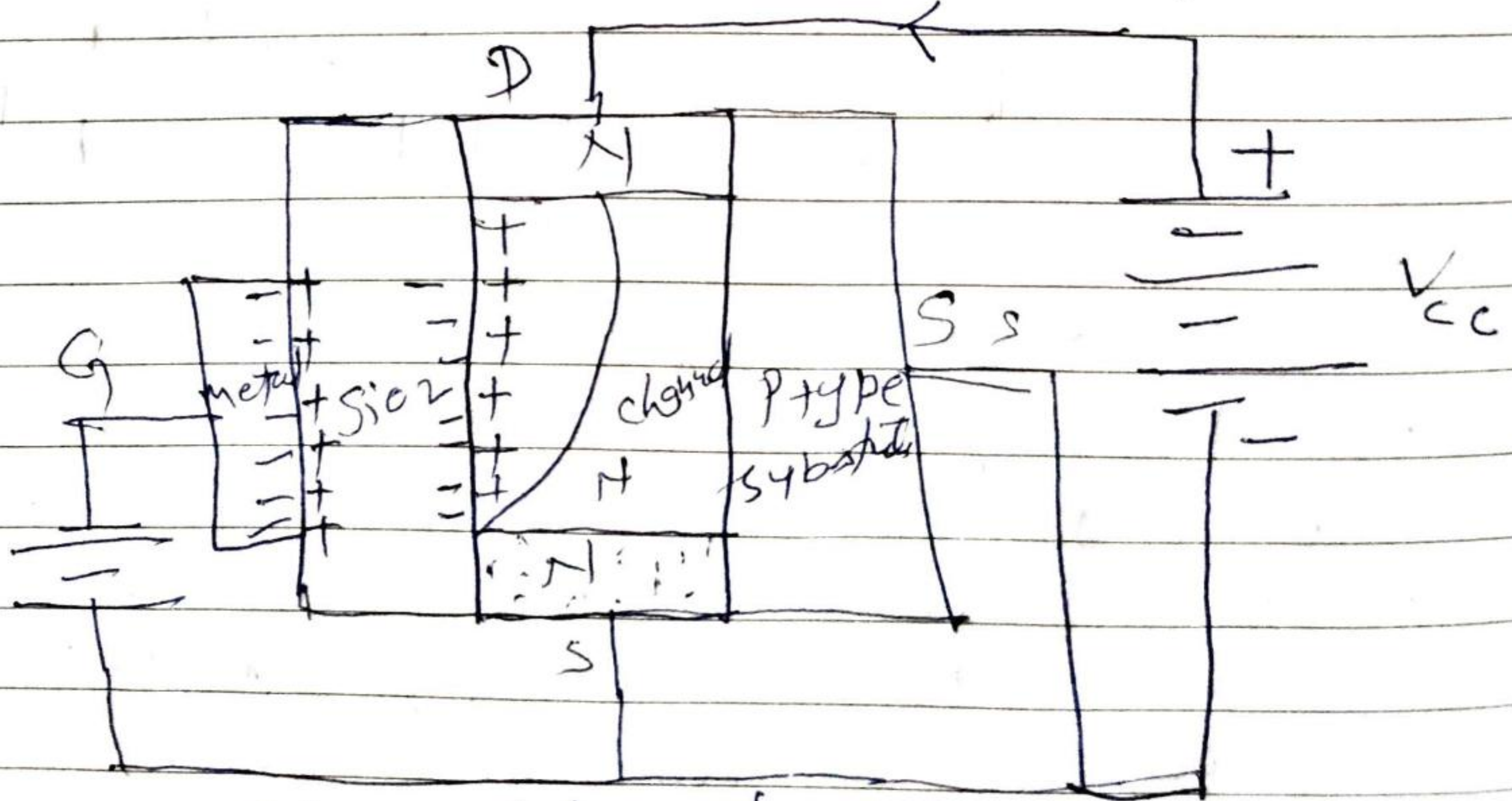
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thin metal layer is deposited

on the oxide layer. This serves as a gate. The oxide layer acts as an insulator between the surface of substrate and the metallic layer. Thus a parallel plate capacitor is formed in which the substrate and metallic layer act as plates while the oxide layer forms the dielectric medium. The gate looks like a metal plate, the arrow is towards N-channel. When SS is connected to an external circuit, shorted to S, MOSFET becomes a 3-terminal device. operation → The substrate, due to lightly doped is usually connected to source, when no gate bias V_{gs} is applied and the drain



Circuit diagram of N-channel MOSFET

source by positive V_{DS} in the majority charge carriers, i.e. electrons flow from source to drain D through the channel. This gives rise to the conventional drain current I_D from D to S . Since the gate is short-circuited to source S , V_{GS} is negative with respect to drain D . The channel is depleted of its electrons due to induced positive charge in it. When V_{DS} is increased, the drain current increases and at a particular value the drain current becomes saturated that value is called pinch off voltage.

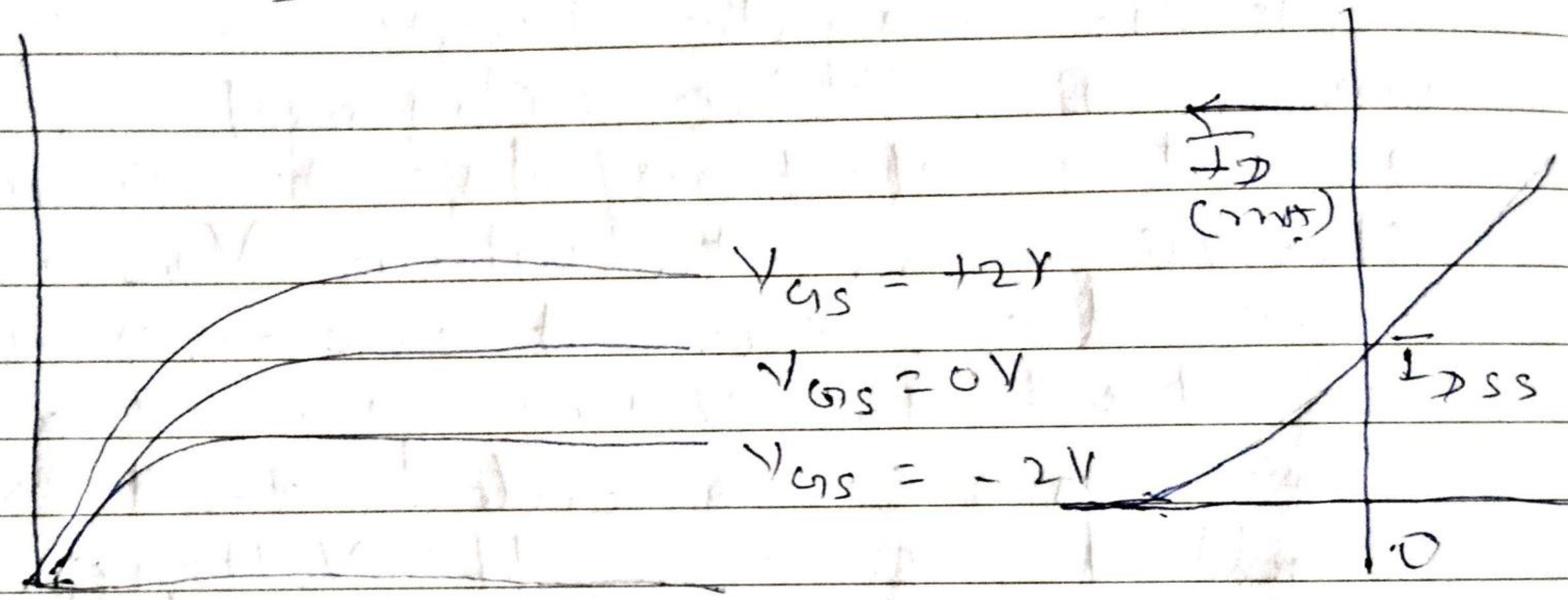
When the gate is given a negative potential with respect to source, the thickness of the depletion region further increases due to further increase of induced positive charge. This causes the reduction in the majority electrons in the channel and consequently the drain current decreases. When the negative gate voltage is sufficiently increased, the channel is pinched off and the drain current becomes zero. When the gate is biased positively with respect to source, the negative charge is

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electrons are induced in the channel which increasing the majority carriers and in the channel hence the drain current, when drain voltage V_{DS} is increased, the current increases and is more than that for V_{GS} .
 $I_D - V_{DS}$ curves \rightarrow



output characteristic

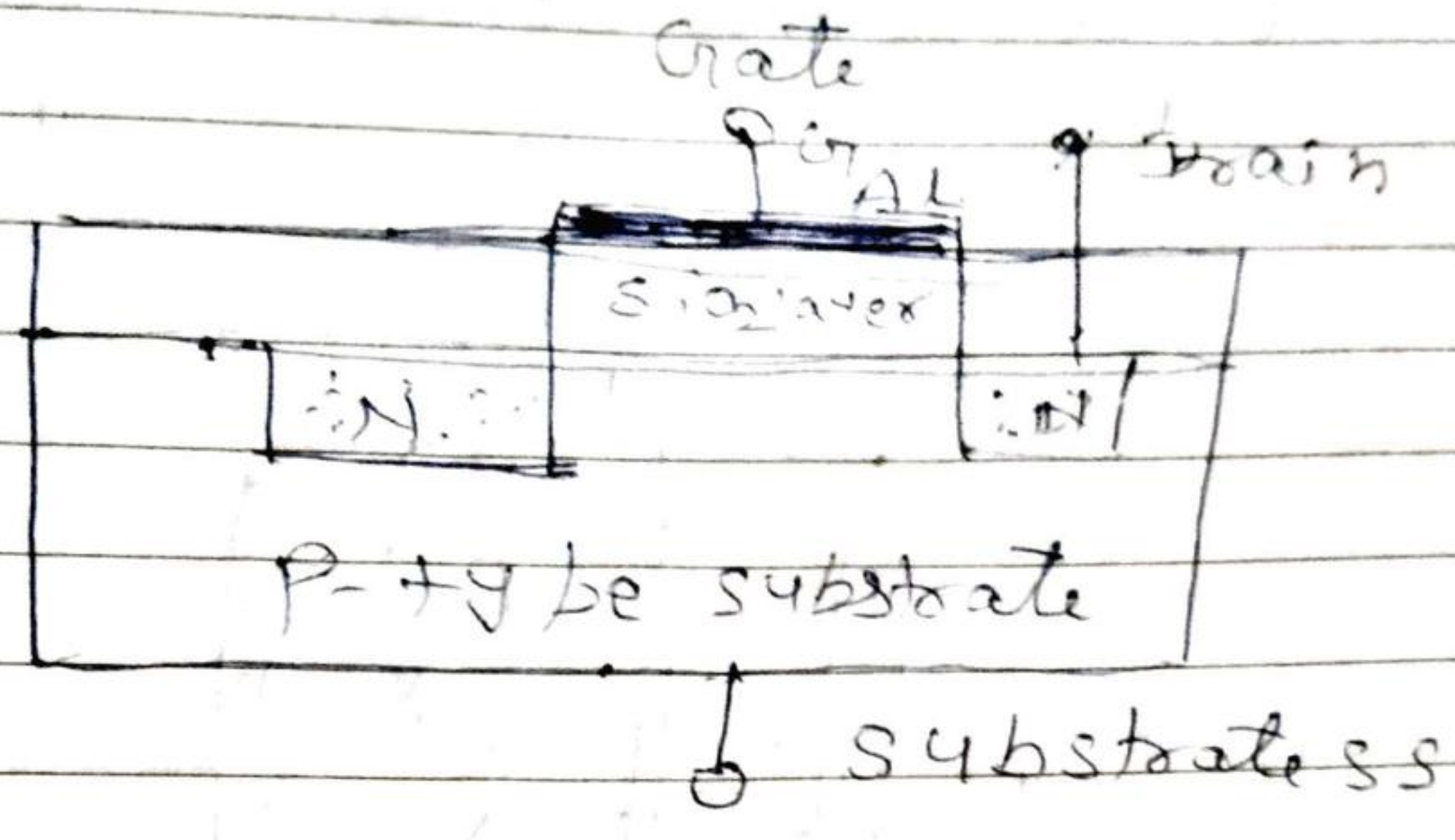
Transfer characteristics \rightarrow when V_{DS} is at constant positive and gate bias V_{GS} is varied the drain current changes.

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SUNDAY

En Abancement

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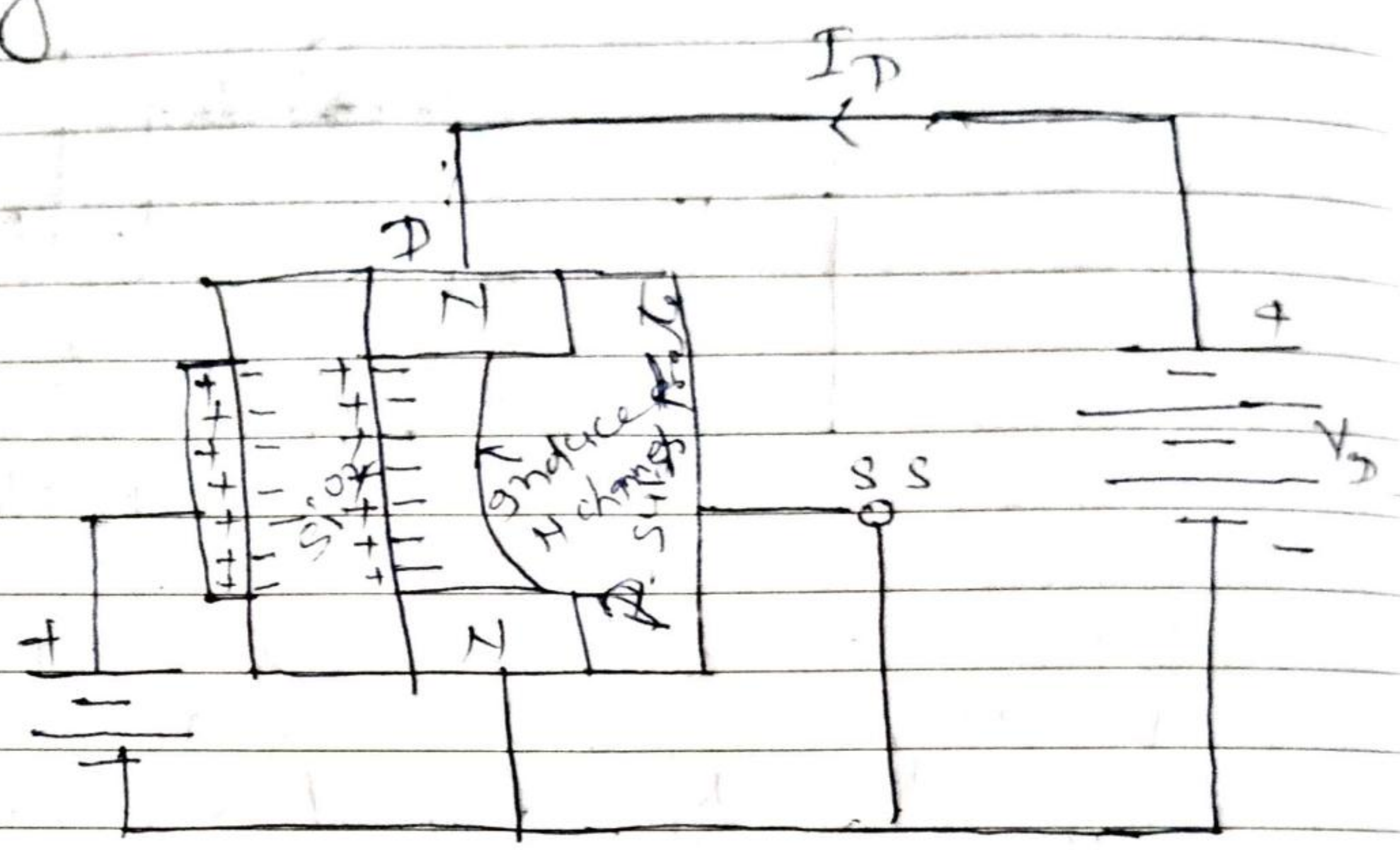


It consists of a lightly doped p-type substrate. In the substrate two highly doped n-regions are diffused to serve as the source and the drain. These regions are separated by a thin layer of insulating silicon-dioxide (SiO_2) grown over the surface then a thin layer is deposited on the oxide layer. This metal layer covers the entire channel region and called gate. The oxide layer acts as an insulator between the surface of substrate and the metallic layer. Thus a parallel plate capacitor is formed in which the substrate and metallic layers act as plates while the oxide layer forms the dielectric medium.

operation \rightarrow The substrate due

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being lightly doped is usually connected to source.



on the substrate two highly doped N-regions are diffused to serve as the source S and the drain D. A thin layer of insulating silicon dioxide (SiO_2) is grown over the surface. Then a thin metal layer is deposited on the oxide layer. This metal layer covers the entire channel region and a gate is formed. The oxide layer acts as an insulator between the surface of substrate and the metallic layer. Thus a parallel plate capacitor is formed in which the substrate and metallic layer act as plates while the oxide layer forms the electric medium.

operation → due to being usually lightly doped is connected to source when gate-source voltage

$V_{gs} = 0$ there is always a reverse biasing junction formed either at the drain or at the source w.r to polarity of drain-source voltage.

There are two P-N junctions formed, one between source S and substrate SS while the other between drain D and substrate SS. Therefore when gate-source voltage $V_{gs} = 0$

No drain current flows (A small leakage current present)

when positive potential is applied at the gate with respect to substrate, negative charges are induced on the semiconductor side. The negative charges induced on a p-type substrate consist of electrons and forms an effective n-type channel in p-type substrate.

when the positive gate-potential V_{gs} is increased, more negative charges (minority charge carriers for p-type substrate) are induced in the channel and its conductivity increases.

For a constant voltage V_{ds} between drain and source. The drain current I_D flowing from source to

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drain increases as the gate potential V_{gs} is increased. Thus the drain current I_D is enhanced by the positive gate potential and hence the device is called enhancement-type MOSFET.

11 Difference between JFET & MOSFET

JFET

MOSFET

- | | |
|--|--|
| (1) Operated in the depletion mode | (1) Operated in the depletion and enhancement mode. |
| (2) The conductivity of channel is controlled by the transverse electric field across the reverse biased P-N junction. | (2) The conductivity of channel is controlled by the transverse electric field induced across an insulating layer, deposited on the semiconducting material. |
| (3) The gate leakage current is of the order of 10^{-9} A. | (3) It is of the order of 10^{-2} A. |
| (4) Output characteristic flatter. | (4) Output characteristic less flatter. |
| (5) The inter-electrode capacitance of JFET are larger. | (5) The inter-electrode capacitance is independent of bias-voltage and these capacitance are smaller. |
| (6) | |